Claims

[c1] 1. An error correcting logic system comprising:
at least two redundant dynamic logic gates, each dynamic logic gate outputting one of a first logic state and a second logic state, the second logic state being output in response to a logic input signal; and
an interconnecting gate coupled to an output of each redundant dynamic logic gate, the interconnecting gate outputting the second logic state only when all of the redundant logic gates output the second logic state.

[c2] 2. The system of claim 1, wherein the interconnecting gate includes an AND gate.

[c3] 3. The system of claim 2, wherein the AND gate includes a NAND gate coupled to an inverting gate.

[c4] 4. The system of claim 2, wherein each dynamic logic gate includes a combinatorial logic section, a pre-charge section, and an inverting gate positioned downstream of a node connecting the combinatorial logic section and the pre-charge section.

[c5] 5. The system of claim 4, wherein the pre-charge section includes a pre-charge device and a keeper device.

[c6] 6. The system of claim 5, wherein an output of the inverting gate feeds back to the keeper device.

[c7] 7. The system of claim 1, wherein the interconnecting gate includes a NOR gate.

[c8] 8. The system of claim 7, wherein each dynamic logic gate includes a combinatorial logic section and a pre-charge section having a pre-charge

device and a keeper device.

[c9] 9. The system of claim 8, wherein an output of the NOR gate feeds back to the keeper device.

[c10] 10. The system of claim 1, wherein the fault is a negative fault.

[c11] 11. The system of claim 1, wherein the interconnecting gate is a static gate.

[c12] 12. The system of claim 1,wherein each dynamic logic gate is a cascode voltage switch.

[c13] 13. An error correcting logic system comprising:
first means for outputting one of a first logic state and a second logic state, the second logic state being output in response to a logic input signal;
second means for outputting one of the first logic state and the second logic state, the second logic state being output in response to the logic input signal; and
third means for interconnecting outputs of the first means and the second means, and for correcting a fault by outputting the second logic state only when both the first means and the second means output the second logic state.

[c14] 14. A method for correcting a fault in a logic system, the method comprising:
providing a first dynamic logic gate;
providing a second dynamic logic gate that is redundant to the first dynamic logic gate; and
combining outputs of the first and econd dynamic logic gates to correct a

fault in one of the first dynamic logic gate and the second dynamic logic gate.

[c15] 15. The method of claim 14, wherein the combining step includes interconnecting outputs of the first and second dynamic logic gates with an AND gate.

[c16] 16. The method of claim 15, wherein the AND gate includes a NAND gate coupled to an inverting gate.

[c17] 17. The method of claim 14, wherein the combining step includes interconnecting outputs of the first and second dynamic logic gates with a NOR gate.

[c18] 18. The method of claim 14, wherein each dynamic logic gate is a cascode voltage switch.

[c19] 19. The method of claim 14, wherein the fault is a soft error.

[c20] 20. The method of claim 14, wherein the combining step includes interconnecting outputs of the first and second dynamic logic gates with a static gate.